Tau™ 2 Electrical Interface Description Document (IDD)

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1 Document

1.1 Revision History

Version	Date	Comments
100	11/07/2011	Initial Release

1.2 Scope

Tau ™ is a miniature infrared imaging core from FLIR Systems®. This Interface Description Document (IDD) defines electrical interface requirements for the Tau 2 configuration of the product.

Note: A number of expansion cards intended for specific applications are available for Tau. In most cases, these expansion cards modify or augment the standard core interfaces. This IDD only applies to the standalone core.

2 Applicable Documents

The following documents form a part of this specification to the extent specified herein.

2.1 FLIR Systems Documents

102-PS242-40	Tau 2 Product Specification
102-PS242-43	Tau 2 / Quark Software Interface Description Document

2.2 External Documents

ANSI/TIA/EIA-232 (formerly RS232)	Interface Between Data Terminal Equipment and Data Circuit-Terminating Equipment Employing Serial Binary Data Interchange
ANSI/TIA/EIA-644	Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits
EIA-170A	Composite Analog Video Signal – NTSC for Studio Applications
ITU Rec. BT.656	Interface for digital component video signals in 525-line and 625-line television systems operating at the 4:2:2 level of Recommendation ITU-R BT.601

3 Electrical Interface Requirements

This document defines requirements for the following Tau 2 interfaces:

- Power
  - Input power
  - 3.3V output
- Analog video data
- Digital video data
  - Parallel channel (single-ended)
  - Serial channel (LVDS)
- Discrete I/O (user-configurable)
- Frame-sync interface (optional)
- Communication interface

3.1.1 Interface Connector

a. The electrical interface to the Tau 2 core is via a single high-density 50-pin connector: Hirose #DF12-50DS-0.5V(86). The recommended mating connector is Hirose #DF12(5.0)-50DP-0.5V(86) for a mating stack height of 5mm.

b. Pin definitions are shown in Table 1. See Figure 1 for a picture showing the pin numbering of the connector. The pin-out is backwards-compatible with Tau 1.X configurations. In other words, a Tau 2.0 can be plugged into the same socket as a Tau 1.X core and will generally operate identically with one exception: for all Tau 2 configurations, the LVDS protocol employs two data lines (see 3.1.4.3) whereas for Tau 1.5 (324x256 configuration), the LVDS protocol employed a single data line.

c. The pins defined as “XP” in Table 1 are reconfigurable by the user. Table 2 shows the pin assignments of the XP bus as a function of selected XP mode.

Table 1: Primary I/O Connector Pin Definition

Pin #	Signal Name	Pin #	Signal Name
1	RS232_TX (see 3.1.7)	2	RS232_RX (see 3.1.7)
3	XP_D17	4	XP_D16
5	DGND	6	DGND
7	Reserved	8	Reserved
9	LVDS_CLK_P (see 3.1.4.3)	10	LVDS_CLK_N (see 3.1.4.3)
11	LVDS_SYNC_P (see 3.1.4.3)	12	LVDS_SYNC_N (see 3.1.4.3)
13	LVDS_DATA1_P (see 3.1.4.3)	14	LVDS_DATA1_N (see 3.1.4.3)
15	LVDS_DATA2_P (see 3.1.4.3)	16	LVDS_DATA2_N (see 3.1.4.3)
17	DGND	18	DGND
19	XP_D15	20	XP_D14
21	XP_D13	22	XP_D12
23	XP_D11	24	XP_D10
25	XP_D9	26	XP_D8
27	DGND	28	DGND
29	XP_D7	30	XPD_6
31	XP_D5	32	XPD_4
33	XP_D3	34	XPD_2
35	XP_D1	36	XPD_0
37	DGND	38	DGND
39	XP_CLK_OUT	40	Reserved
41	DGND	42	DGND
43	VIDEO_H (see 3.1.3)	44	VIDEO_L (see 3.1.3)
45	DGND	46	3V3_OUT (see 3.1.2)
47	MAIN_PWR_RTN (see 3.1.2)	48	MAIN_PWR (see 3.1.2)
49	MAIN_PWR_RTN (see 3.1.2)	50	MAIN_PWR (see 3.1.2)

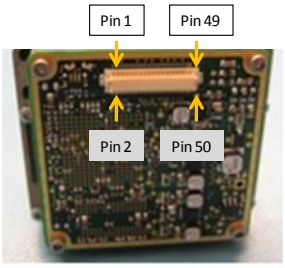


Figure 1: Primary I/O Connector Pinout, Hirose #DF12-50DS-0.5V(86)

Table 2: XP Bus Reconfigurable Pins

XP1 Bus Signal	Pin #	XP1 Mode (Field-Selectable)			
		BT.656 (see 0)	CMOS 14-bit (see 3.1.4.2)	CMOS 8-bit (see 3.1.4.2)	Data Disabled
XP_CLKOUT	39	BT656_CLK	CMOS_CLK	CMOS_CLK	z
XP_D0	36	BT656_D0	CMOS_D0	CMOS_D0	z
XP_D1	35	BT656_D1	CMOS_D1	CMOS_D1	z
XP_D2	34	BT656_D2	CMOS_D2	CMOS_D2	z
XP_D3	33	BT656_D3	CMOS_D3	CMOS_D3	z
XP_D4	32	BT656_D4	CMOS_D4	CMOS_D4	z
XP_D5	31	BT656_D5	CMOS_D5	CMOS_D5	z
XP_D6	30	BT656_D6	CMOS_D6	CMOS_D6	z
XP_D7	29	BT656_D7	CMOS_D7	CMOS_D7	z
XP_D8	26	DISCRETE5	CMOS_D8	DISCRETE5	DISCRETE5
XP_D9	25	DISCRETE4	CMOS_D9	DISCRETE4	DISCRETE4
XP_D10	24	DISCRETE3	CMOS_D10	DISCRETE3	DISCRETE3
XP_D11	23	DISCRETE2	CMOS_D11	DISCRETE2	DISCRETE2
XP_D12	22	z	CMOS_D12	z	z
XP_D13	21	EXT_SYNC	EXT_SYNC	EXT_SYNC	EXT_SYNC
XP_D14	20	DISCRETE1	CMOS_D13	DISCRETE1	DISCRETE1
XP_D15	19	DISCRETE0	DISCRETE0	DISCRETE0	DISCRETE0
XP_D16	4	DISCRETE_7	CMOS_FRAME_VALID	CMOS_FRAME_VALID	DISCRETE7
XP_D17	3	DISCRETE_6	CMOS_LINE_VALID	CMOS_LINE_VALID	DISCRETE_6

Note: Purple font = output signal. Blue font = Input or Output. z = high impedance

3.1.2 Power Interface

a. The Tau 2 core provides full functionality when voltage as specified in Table 3 is applied across MAIN_PWR and MAIN_PWR_RTN.

b. For input voltage between the minimum value and the shutdown value specified in Table 3, core behavior is undefined. The Tau 2 core may reset continuously or may power down.

Note: The core does not provide internal protection against reverse-voltage or over-voltage.

Table 3: Tau 2 Input Power Requirements

Parameter	Value	Notes
Maximum voltage	6.0V	*Voltage in excess of this value may cause permanent damage to the core.*
Minimum voltage	4.0V or 4.4V	*The 4.0V requirement applies to the shutterless and standard shutter configs. The 4.4V requirement applies to the iris-style shutter configs.*
Shutdown voltage	0.0V - 3.8V	*See item b above.*
Average Power Dissipation	See below.	*Varies by configuration and varies over temperature*
Surge current at start-up	< 600 mA	*Duration < 8 msec*
Max. current after start-up (during shutter cycle)	< 450 mA	

Table 4: Tau 2 Power Dissipation

Tau 2 Configuration	Power at 25C	Power at 80C
324 / 336	≤ 1.00W	≤ 1.15W
640	≤ 1.10W	≤ 1.25W

Note: The values above assume a single digital channel (BT.656, CMOS, or LVDS) is enabled and that the analog channel is disabled. The values are increased by approximately 65 mW by disabling all digital channels and instead enabling analog.

c. The Tau 2 core provides an output voltage with characteristics as specified in Table 5 between the 3V3_OUT and DGND pins. This voltage is intended primarily for powering expansion electronics designed by FLIR Systems but may be applicable for other use.

Note: Loading down this voltage in excess of the peak supply current specified in Table 5 may cause the core to reset or behave unpredictably.

Table 5: 3V3 Characteristics

Parameter	Value
Voltage range	3.3V ± 3%
Peak supply current	100 mA

3.1.3 Analog Video Channel

a. The Tau 2 core provides analog video on the signals named VIDEO_H and VIDEO_L. Figure 2 shows required termination of the analog video channel. For transmission of the video channel, a coaxial cable with 75 ohm characteristic impedance is required.

b. The timing and voltage level of the analog video signal complies with either NTSC or PAL protocol. The choice between NTSC or PAL is field-selectable (via the serial comm. interface).

c. The channel may be disabled for a savings of approximately 75 mW.

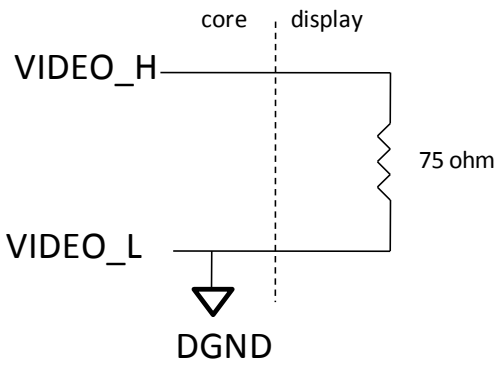


Figure 2: Required Termination of the Analog Channel

3.1.4 Digital Data Channels

a. The Tau 2 core provides the option of two simultaneous digital output channels, one parallel and one serial.

b. One or both channels can be disabled for a power savings of approximately 10 mW per channel.

c. The parallel channel can be field-configured to provide data via BT.656 protocol or a CMOS protocol, defined further in 0 and 3.1.4.2, respectively. Maximum recommended transmission length is approximately 1 m.

d. The serial port employs an LVDS protocol further defined in 3.1.4.3. Maximum recommended transmission length is approximately 3 m.

Note: Because the BT.656 and CMOS outputs are provided on a reconfigurable XP Bus available to multiple interface types / data rates, external signal filtering is required to minimize radiated emissions. For a specific XP-bus configuration and customer application, signal and power filtering should be tailored when targeting a given EMI specification. It is recommended that filtering be located immediately after the Tau mating connector. The filter type should address the extended harmonic frequencies of the XP Bus signaling and not cripple the signal shape and timing. The filter could be in the form of a series resistor or ferrite bead. The Tau chassis provides a flat metallic surface and four (4) mounting screw locations to fasten a mating PCB or Flex PCB. This surrounding chassis-attachment concept is the same as a cable shield.

3.1.4.1 BT.656 Protocol

The Tau 2 core provides the option of configuring the XP bus to output digital data with timing/format in compliance with ITU Recommendation BT.656.

Note: This interface is fully compliant with the Recommendation except in terms of line driver characteristics, ECL-compatibility, and connector type.

1. The channel consists of a clock and 8 parallel bits of data, transmitted via single-ended 3.3V CMOS logic levels. See Table 2 for pin assignments.
2. The channel can only be configured for 8-bit (post-AGC) data. Symbol overlay and YCbCr encoding is included in this output. (It is the only of the digital output options that includes symbol overlay and color encoding.)
3. Clock frequency is 27 MHz. Refer to the ITU Recommendation for detailed timing / format requirements.
4. Frame rate is 29.97 Hz (NTSC) or 25.00 Hz (PAL). For "fast" 324 and 336 configurations, each data field is duplicated once (i.e., 2 fields per frame) whenever the averager feature is enabled. (See the Tau 2 Product Specification for more information on fast and slow configurations and the averager feature.) For the fast 640 configurations and for the fast 324 / 336 configurations with the averager disabled, each BT.656 field contains unique data.
5. For "slow" configurations, each data field is duplicated multiple times to produce an *effective* frame rate $\leq$ 9Hz.

3.1.4.2 CMOS Protocol

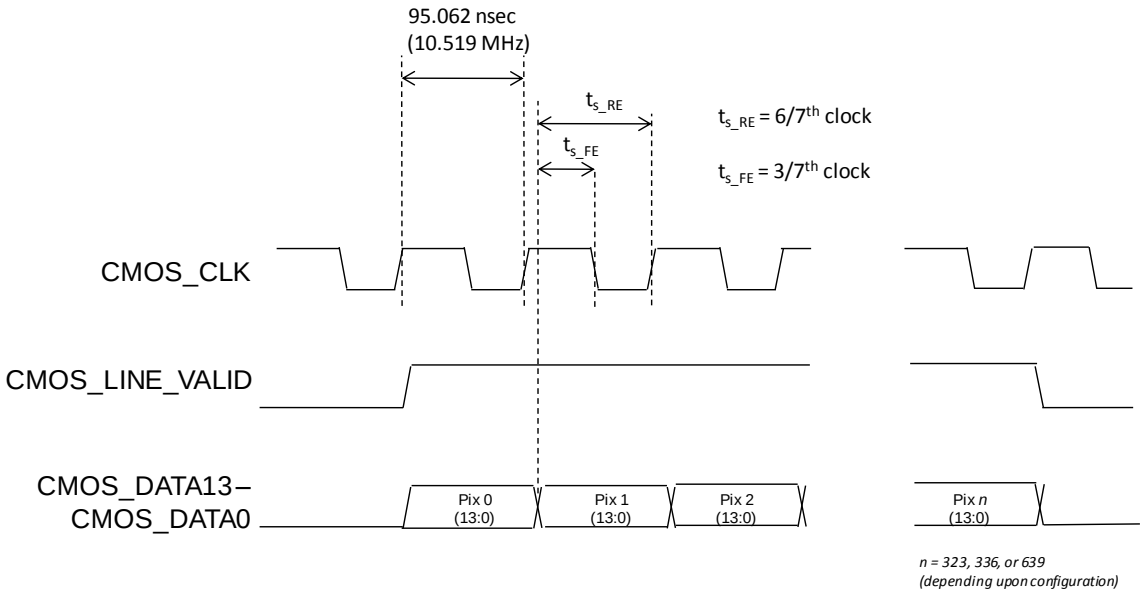
The Tau 2 core provides the option of configuring the XP bus to output a digital data protocol resembling that of a typical CMOS camera. Specifically:

1. The channel consists of a clock, up to 14 parallel bits of data, a line-valid signal, and a frame-valid signal. The channel utilizes 3.3V CMOS logic levels. See Table 2 for pin assignments.
2. The choice between 14-bit (pre-AGC) or 8-bit (post-AGC) data is field-selectable.
3. Line timing is depicted in Figure 3. The clock rate is 10.519 MHz.
4. Frame timing is depicted in Figure 4. The frame rate depends upon configuration and settings as shown in Table 6.
5. No data output is output on the CMOS channel during each flat-field correction (FFC) period. That is, LINE_VALID, DATA_VALID, and CMOS_DATA[0-13] are all disabled throughout FFC.

Table 6: Frame Rate vs. Configuration / Settings

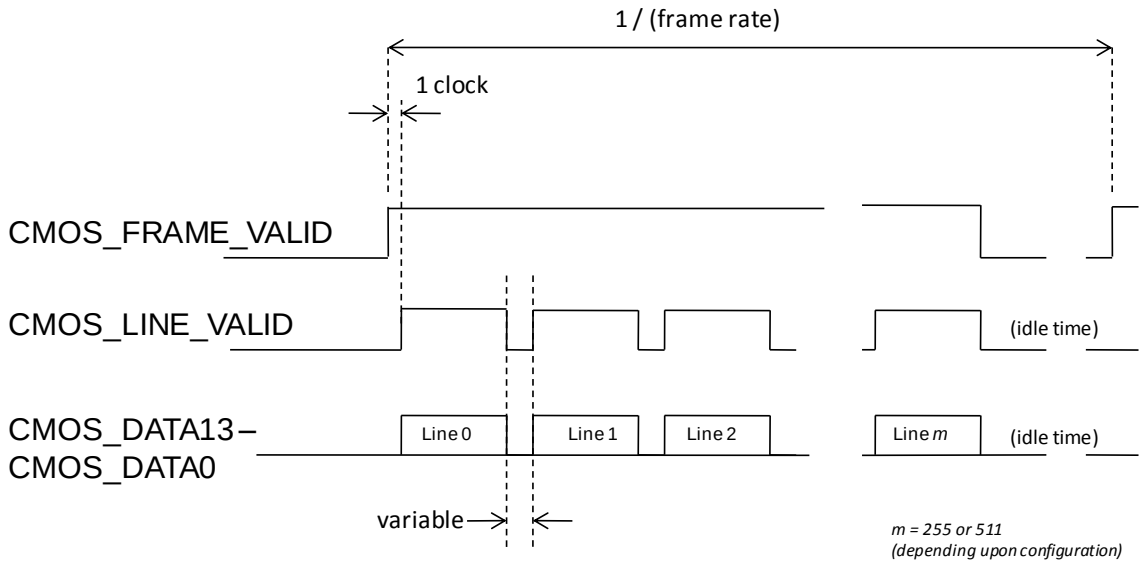
Configuration, Video Speed	Configuration, Resolution	Video Setting	Averager Mode	Frame Rate (Hz)
Fast	324 /336	NTSC	Disabled	59.94 Hz
Fast	324 /336	PAL	Disabled	50.00 Hz
Fast	324 /336	NTSC	Enabled	29.97 Hz
Fast	324 /336	PAL	Enabled	25.00 Hz
Fast	640	NTSC	not applicable	29.97 Hz
Fast	640	PAL	not applicable	25.00 Hz
Slow	324 /336	NTSC	Disabled	8.56 Hz
Slow	324 /336	PAL	Disabled	8.33 Hz
Slow	324 /336	NTSC	Enabled	7.49 Hz
Slow	324 /336	PAL	Enabled	8.33 Hz
Slow	640	NTSC	not applicable	7.49 Hz
Slow	640	PAL	not applicable	8.33 Hz

- *Note 1: The resolution value listed in the above table is that shown in the part number of the Tau 2 core. See the Tau 2 Product Specification for further description. It refers to the number of pixel columns.*
- *Note 2: See the Tau 2 Product Specification for a description of the averager feature. The 640 configurations do not provide this feature.*
- *Note 3: The idle time at the end of each frame varies considerably depending upon frame rate and number of pixels per frame.*



Note: Figure is not necessarily to scale. CLK duty cycle is 4/7. Data may be latched on the rising or falling edge of CLK.

Figure 3: Line Timing, CMOS Protocol



Note: Figure is not to scale.

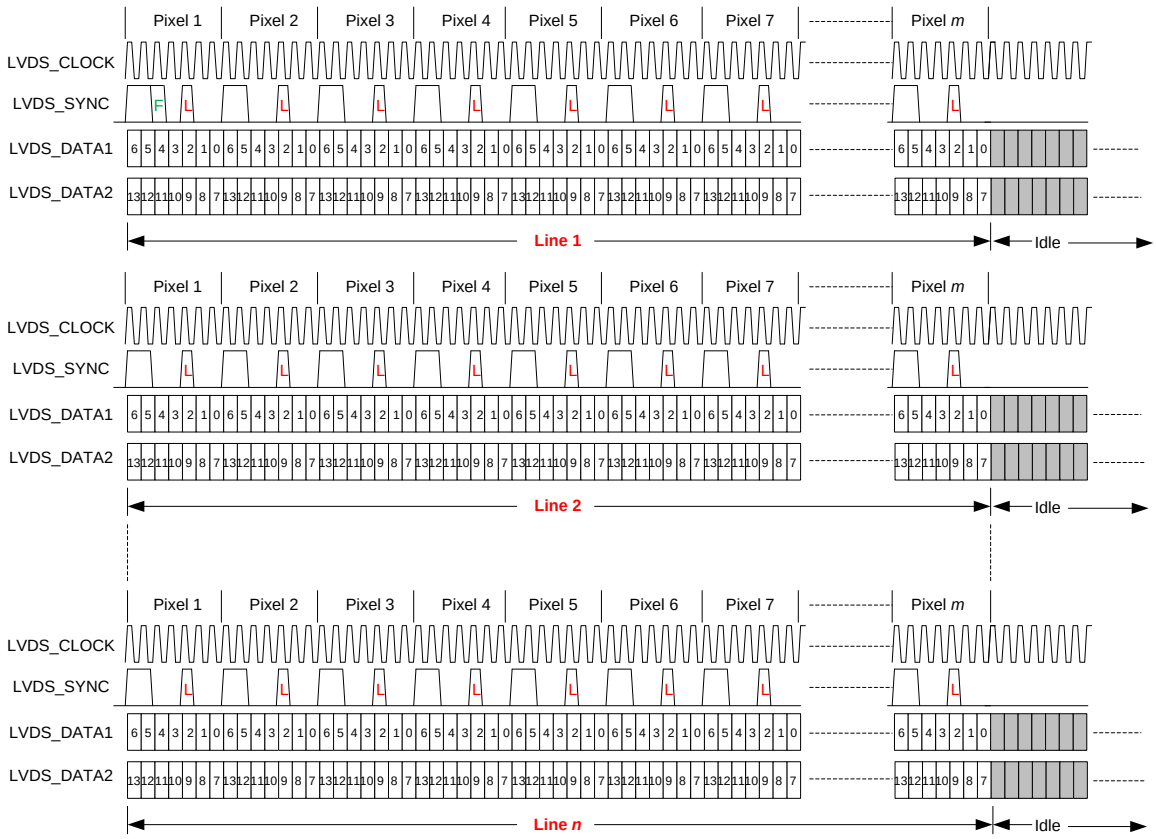
Figure 4: Frame Timing, CMOS Protocol

3.1.4.3 LVDS Protocol

The Tau 2 core provides the option of a digital data protocol used on previous FLIR products including Photon and Tau. Specifically:

1. The channel consists of a clock pair, an encoded sync pair, and two data-line pairs. See Table 1 for pin assignments. All signals employ low-voltage differential signaling (LVDS).
2. The choice between 14-bit or 8-bit data is field-selectable. For this channel, 8-bit video does not include symbol overlay.
3. The clock rate is 73.636 MHz. One pixel datum is transmitted in each 7-clock period. Line timing and sync encoding of all configurations are shown in Figure 5. Phasing of the clock relative to the sync and data signals is shown in Figure 6.

   Note: In the original Tau 320 configuration, only a single data line was employed on the LVDS interface. For Tau 2, all configurations utilize two data lines regardless of number of pixels.
4. The frame rate is identical to that of the CMOS channel as shown in Table 6 .
6. No data output is output on the LVDS channel during each FFC period. That is, LVDS_SYNC, and LVDS_DATA are both disabled throughout FFC.



Notes:

F = frame sync; logic high on the first word starting the first line, logic low otherwise

L = line sync; logic high during valid pixel data, logic low otherwise

Figure 5: Digital Data Timing, LVDS Protocol, all Tau 2 Configurations

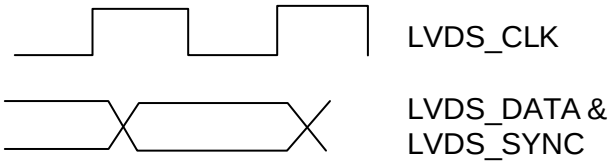


Figure 6: Digital Data Timing, LVDS Clock relative to Data and Sync

3.1.5 Configurable Discrete I/O Pins

Depending upon the XP bus mode (see Table 2), the Tau 2 core provides up to 8 signals referred to as discrete I/O pins (DISCRETE0 – DISCRETE7) that can each be field-configured to provide a specified functionality when shorted to DGND. For example, one of the pins might be configured to toggle between white hot and black hot polarity. The full list of functions that can be assigned to these pins is defined in the Tau 2 Product Specification. There is no de-bounce circuitry on the signals. They are polled at 30Hz.

3.1.6 Frame Synchronization Interface

The Tau 2 core provides the option of transmitting or receiving a frame-synchronization pulse on EXT_SYNC. This feature provides the capability to synchronize frame start between two cores, one configured as master and the other configured as slave, or to synchronize the Tau 2 core with a different camera. Note that the synchronization state (master, slave, or disabled) must be preconfigured prior to power-up (i.e., the camera must be re-started after changing the mode and saving as a power-on default).

3.1.6.1 Master Mode

When configured as a master, the core transmits a pulse on the frame-synchronization interface at a rate of once per frame (29.97Hz for NTSC, 25.00 Hz for PAL). The pulse complies with the characteristics defined in Table 7.

Table 7: Sync Pulse Characteristics

Mode	Signal Direction	Voltage (relative to DGN)	Frequency Range	Pulse width (minimum)
Master	Output	3.3V	29.97 NTSC, 25.00 PAL	100 nsec
Slave NTSC	Input	3.3V	15Hz to 29.98Hz	100 nsec
Slave PAL	Input	3.3V	12.5Hz to 27.25Hz	100 nsec
Disabled	n/a	3.3V	n/a	n/a

3.1.6.2 Slave Mode

When configured as a slave, the core synchronizes the FPA frame start to the rising edge of a pulse received on the frame-synchronization interface. The required frequency and pulse width are defined in Table 7. Any pulses sent at a rate greater than 30Hz will be ignored. (For example, if pulses are sent at 40 Hz (25 msec period), the pulse sent 25 msec after the first will be ignored. The next frame will be triggered on the next pulse for an effective frame rate of 20 Hz.) When in slave mode, the core will not output data until a valid pulse is received.

Note 1: For a core configured as a slave, proper analog video output requires that the pulse timing be sent at a rate confirming to the selected video standard (either NTSC or PAL).

Note 2: The LVDS / CMOS frame sync signals are delayed relative to the External-Frame-Sync pulse. Consequently, digital frame acquisitions should use the appropriate sync signal and not rely on the External Frame Sync pulse for synchronization.

For slow configurations, the output frame rate is a fraction of the sync pulse rate. Because there is ambiguity as to which received pulse triggers the frame timing, FLIR does not recommended to use the external sync interface with a slow-configured Tau 2 core.

3.1.7 Communication Channel

The Tau 2 core provides an asynchronous serial interface consisting of the signals named RS232_RX (input to core), RS232_TX (output from core), and DGND. The interface complies with the RS232 standard except in voltage levels: 3.3V CMOS signal levels are employed. The Tau 2 core automatically detects the polarity of incoming messages (standard logic or inverted logic) and replies at the same polarity. The Tau 2 is capable of communication at various baud rates, as further described in the Tau 2 Software IDD. The communication protocol of the RS232 channel is also defined in the Tau 2 Software IDD.

If you have questions that are not covered in this manual, or need service, contact FLIR Commercial Systems Customer Support at 805.964.9797 for additional information prior to returning a camera.

This documentation and the requirements specified herein are subject to change without notice.

This equipment must be disposed of as electronic waste.
Contact your nearest FLIR Commercial Systems, Inc. representative for instructions on how to return the product to FLIR for proper disposal.

FCC Notice. This device is a subassembly designed for incorporation into other products in order to provide an infrared camera function. It is not an end-product fit for consumer use. When incorporated into a host device, the end-product will generate, use, and radiate radio frequency energy that may cause radio interference. As such, the end-product incorporating this subassembly must be tested and approved under the rules of the Federal Communications Commission (FCC) before the end-product may be offered for sale or lease, advertised, imported, sold, or leased in the United States. The FCC regulations are designed to provide reasonable protection against interference to radio communications. See 47 C.F.R. §§ 2.803 and 15.1 et seq.

Industry Canada Notice. This device is a subassembly designed for incorporation into other products in order to provide an infrared camera function. It is not an end-product fit for consumer use. When incorporated into a host device, the end-product will generate, use, and radiate radio frequency energy that may cause radio interference. As such, the end-product incorporating this subassembly must be tested for compliance with the Interference-Causing Equipment Standard, Digital Apparatus, ICES-003, of Industry Canada before the product incorporating this device may be: manufactured or offered for sale or lease, imported, distributed, sold, or leased in Canada.

Avis d'Industrie Canada. Cet appareil est un sous-ensemble conçu pour être intégré à un autre produit afin de fournir une fonction de caméra infrarouge. Ce n'est pas un produit final destiné aux consommateurs. Une fois intégré à un dispositif hôte, le produit final va générer, utiliser et émettre de l'énergie radiofréquence qui pourrait provoquer de l'interférence radio. En tant que tel, le produit final intégrant ce sous-ensemble doit être testé pour en vérifier la conformité avec la Norme sur le matériel brouilleur pour les appareils numériques (NMB-003) d'Industrie Canada avant que le produit intégrant ce dispositif puisse être fabriqué, mis en vente ou en location, importé, distribué, vendu ou loué au Canada.

EU Notice. This device is a subassembly or component intended only for product evaluation, development or incorporation into other products in order to provide an infrared camera function. It is not a finished end-product fit for general consumer use. Persons handling this device must have appropriate electronics training and observe good engineering practice standards. As such, this product does not fall within the scope of the European Union (EU) directives regarding electromagnetic compatibility (EMC). Any end-product intended for general consumer use that incorporates this device must be tested in accordance and comply with all applicable EU EMC and other relevant directives.